BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER

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FIELD OF THE INVENTION

This invention relates to a method and structure for making an interconnect between a device layer and a handle wafer which forms the substrate through a buried oxide for bonded silicon on insulator (SOI) structures.

BRIEF DESCRIPTION OF THE PRIOR ART

In the fabrication of bonded SOI devices, the normal process flow includes forming of an electrically insulating layer over a device wafer with bonding of the electrically insulating layer to a handle wafer which forms the substrate. The device wafer is then thinned down to a device level thickness.

It is known that two essentially coplanar surfaces of layers of silicon and/or silicon dioxide which are in contact with each other can be bonded together by first placing the two layers in contact with each other whereby the two layers are held together by van der Waals forces. The bond strength is increased by applying an annealing step which apparently causes some migration of atoms between the two layers in the immediate region of the contacting surfaces to cause the bonding. This procedure has been used to fabricate bonded silicon on insulator (SOI) structures with devices formed in

the device silicon layer separated by a silicon dioxide layer from the substrate silicon layer with each of the silicon layers being coplanar with opposing surfaces of the silicon dioxide layer with the bond interface at either of the silicon/silicon dioxide interfaces or within the silicon dioxide layer. Preferably, the bond interface is at the substrate/silicon dioxide interface. Structures such as interconnect may be included within the silicon dioxide layer, and dopant may be implanted into the substrate through the device and silicon dioxide layers.

In the prior art, whenever connection was to be made between the device layer and the substrate, the procedure has involved initial etching through an area of the device layer with subsequent etching through the electrically insulating layer to the substrate. Interconnect material would then be formed in the etched away region. This procedure takes up device surface area and requires the ability to reliably form the interconnect in the etched vias extending through both the device layer and the electrically insulating layer which can be difficult for thick dielectric layers. In addition, since fabrication takes place from the outer surface of the device layer, it is not possible to have a connection to just the inner surface of the device layer. Furthermore, there is no provision for utilizing the electrically insulating layer for anything other than as a dielectric separator.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a method and structure whereby not only is there provided an easily fabricated interconnect between the device layer and the substrate, but, in addition, there is the capability of providing buried structures within the electrically insulating layer connecting to both the substrate and the device layer without consuming outer surface area of the device layer.

Briefly, a dielectric layer is formed on the handle wafer and/or the device wafer. Interconnect structures are included in the dielectric layer(s), optionally connecting to the device wafer of handle wafer, and optionally extending to the outer surface of the dielectric layer. There is flexibility to form interconnect with high aspect ratio (depth to cross-sectional area) traversing the dielectric layer. Optionally, device and/or alignment structures may be formed in the device wafer, dielectric layer(s), or handle wafer. The bonding surfaces are planarized as necessary, such as with spin on glass (SOG), resist etch back (REB) and/or chemical/mechanical polish (CMP), such that the opposing bonding surfaces are sufficiently conformal so that the van der Wall's forces described above come into play when the wafers are aligned and brought into close proximity. The bonding step then takes place by standard techniques. A portion of the device wafer is removed to provide the desired device layer thickness, again by standard techniques. Devices are then formed in the device layer.

In the above, a portion of the interconnect structure in the dielectric layer is completed at the bonding interface. Preferably, the bonding interface is between the dielectric layer and the handle wafer, and connection is made from an interconnect structure in the dielectric layer to the handle wafer. Optionally, the bonding interface is

between the dielectric layer and the device wafer, and connection is made from an interconnect structure in the dielectric layer to the device wafer. As a further option, the bonding interface is between a dielectric layer formed on the device wafer and a dielectric layer formed on the handle wafer, and connection is made between interconnect structures in each of the dielectric layers. In each case, optionally, a thin dielectric layer may be formed between an interconnect structure and the bonding interface, either inadvertently or to facilitate bonding. Then a sufficiently high voltage is applied across this thin dielectric to cause breakdown and completion of the interconnection. The voltage can be applied at any point after the bonding, including immediately after bonding, after device wafer thinning, after initial patterning of the device layer, and after packaging of the completed integrated circuit.

It can be seen that, in accordance with the current invention, there is provided a method for fabrication of SOI structures wherein electrical connection can be made across a bonding interface without requiring etching through the outer surface of the device layer. Further, there is flexibility in forming an interconnect traversing the dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a cross sectional view of a first embodiment of a structure fabricated in accordance with the present invention;

FIGURE 2 is a cross sectional view of a second embodiment of a structure fabricated in accordance with the present invention;

FIGURE 3 is a cross sectional view in accordance with a second embodiment of the present invention;

FIGURE 4 is a cross sectional view in accordance with a third embodiment of the present invention;

FIGURE 5 is a cross sectional view in accordance with a fourth embodiment of the present invention; and

FIGURE 6 is a cross sectional view of a subsequent portion of the process flow in fabrication of the embodiments of FIGURES 4 and 5.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring first to FIGURE 1, there is shown an SOI structure in accordance with a first embodiment of the present invention. The structure includes a handle wafer 1 which forms the substrate, and electrically insulating layer 3. Optionally, the dielectric layer 3 is formed in the handle wafer and bonded to the device wafer, or formed on the device wafer and bonded to the handle wafer. The device wafer 5 and the substrate 1 may have active and/or passive devices formed therein optionally making connection to an interconnect in the electrically insulating layer. The electrically insulating layer 3 may include therein interconnect structures 7 interconnecting the device wafer 5 to the substrate 1. The electrically insulating layer 3 can also have, with or without the above described interconnect structure, passive elements 9, such as, for example, inductors, with an interconnect 11 to the device wafer 5 and/or the substrate 1 to the passive elements.

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The structure of FIGURE 1 is fabricated by providing each of a handle wafer 1 and a device wafer 5. A dielectric layer 3 is formed on one of handle wafer 1 or device wafer 5, with interconnect extending to the outer surface of dielectric 3 with or without an interconnect passing entirely therethrough 7 and/or one or more passive elements buried therein 9 and/or on a surface thereof (not shown) and/or interconnect 11 between the passive elements and one or both opposed surfaces of the electrically insulating layer. A1 Optionally, alignment marks are formed in the dielectric layer 3 and/or in the device wafer 5 and/or the handle wafer 1. The outer surface of dielectric layer 3 is planarized, such as with combined use of a flowable dielectric and CMP. The interconnect initially extending to the outer surface of dielectric layer 3 is optionally covered with a thin dielectric after planarization. Also, a thin dielectric, such as a native oxide, may be

formed on the wafer to which dielectric layer 3 is to be bonded. The one of handle wafer 1 or device wafer 5 on which the dielectric is formed is then bonded to the other of the device wafer and handle wafer by standard means. The device layer 5 is then thinned back to the phantom line 13 with fabrication then continuing in standard manner to provide a completed device. The interconnect 7 will generally contact to source, drain or body regions of the device subsequently fabricated in device layer 5, or to interconnect formed on the outer surface of device layer 5. In the event a thin native oxide has developed over the device wafer 5 or the substrate 1 or the flowable dielectric insulates the interconnect in the electrically insulating layer from the substrate or device wafer, a sufficiently high voltage can be passed through the circuitry involving the interconnect 7 to cause breakdown of the native oxide or other dielectric and allow completion of the connection as is well known in the art. Optionally, the voltage can be applied prior to completion of fabrication of devices in device layer 5.

Referring to FIGURE 2 wherein like reference numbers refer to the same or similar structures, there is shown a structure which is the same as in FIGURE 1 and fabricated in the same manner except that the device layer includes a mesa portion 15 of the device wafer 5' which extends through the electrically insulating layer 3' and makes contact with the substrate 1. Connection can be made directly between the substrate 1 and the device wafer 5 as well as through the electrically insulating layer 3. As shown, other interconnection between the device wafer 5' and the substrate 1 can be made with an interconnect 7 as in FIGURE 1 and other interconnect 11 and/or passive elements 9 can be formed as discussed above with reference to FIGURE 1.

For the structure of FIGURE 2, silicon-to-silicon bonding can be accomplished simultaneously with the dielectric to silicon bonding. Optionally, a thin oxide may be formed in region 17 prior to bonding and subsequently broken down with application of a sufficiently high voltage.

Formation of a via through a relatively thick dielectric layer as may be used for the dielectric layer between the device wafer and the handle wafer can be difficult with standard process techniques. Forming a via or vias 7 through the dielectric 3 prior to bonding provides flexibility. One option is to form the dielectric 3 in layers with multiple levels of interconnect 11 as illustrated in FIGURE 3. Another alternative is illustrated in FIGURES 4 and 5. Dielectric layer 3 is formed, and a pattern is etched through the dielectric layer 3 to the underlying device wafer 5, forming an edge 21 where the via is to be. A sidewall of interconnect material 23 is formed on the edge as illustrated in FIGURES 4 and 5. The sidewall 23 is then selectively etched, if required, using patterned resist, leaving the interconnect material at the via location as illustrated in FIGURES 4 and 5. Additional dielectric material 25 is subsequently deposited and planarized in the via 7, as illustrated in FIGURE 6.

Various dielectric materials or composites thereof can be used to form layer 3, such as, for example, grown oxides, deposited oxides, and nitrides. Also, various conductive materials can be used to form the interconnect, such as polysilicon, amorphous silicon and tungsten. With low temperature bonding, additional materials, such as aluminum, can be used. Stacked materials, such as tungsten with titanium nitride at the interfaces can also be used. Silicides can be formed at the interconnect to wafer interface.

Though the invention has been described with reference to specific preferred embodiments thereof, many variations and modifications will immediately become apparent to those skilled in the art. For example, the invention may incorporate multiple layers of bonding. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.